a ferroelectric FET, which is provided on the semiconductor substrate and includes a ferroelectric film provided over the semiconductor substrate, a control gate electrode provided on the ferroelectric film and source/drain regions;

a memory circuit block, in which the ferroelectric FET is arranged; and

a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.

56. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

a) forming a gate insulating film and a gate electrode for each of first- and second-channel-type MISFETs and a ferroelectric FET over a semiconductor substrate;

b) implanting ions of a dopant for forming source/drain regions from over the gate electrode of the ferroelectric FET and the gate electrode of one of the first- and second-channel-type MISFETs;

c) implanting ions of another dopant for forming source/drain regions from over the gate electrode of the other MISFET;

d) forming an interlevel dielectric film covering the gate electrodes of the MISFETs and the ferroelectric FET, forming a contact hole, which passes through the interlevel dielectric to reach the gate electrode of the ferroelectric FET, and then filling the contact hole with a conductor material to form a contact member;

e) forming an intermediate electrode, a ferroelectric film and a control gate electrode over the interlevel dielectric film so that the intermediate electrode is connected to the contact member and that the ferroelectric film is in contact with an upper surface of the intermediate electrode and that the control gate electrode faces the intermediate electrode with the ferroelectric film interposed therebetween;

f) forming a memory circuit block, in which the ferroelectric FET is arranged; and

g) forming a control circuit block, in which the MISFET is arranged, for controlling the memory circuit block.